Digital Design Lab
EEN 315 Section 47

Lab 3: Tone Generator

Group #2
Connor McCullough
(Partners: Davis Sprague,
Anthony Taboada,
Joe Barra,
Nick Hetko)

May Lin, TA

University of Miami
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Abstract

The purpose of this lab was to further understanding of multiplexers, flip flops, and K maps by creation of a sequence generator, as well as introducing new concepts such as a modulo N chip, frequency generation using a 555 timer, frequency division, and use of a speaker. The lab also tested integration of all of these techniques on a single board.

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Overview

Requires knowledge of sequential logic and ability to create a sequential circuit using a state diagram. Equations for determining frequency of a 555 timer are required as well. Ability to examine and comprehend IC data sheets and implement a block diagram of integrated circuits.

Objectives

This report will detail the process behind the design and implementation of a tone generator made up of a sequence generator and frequency generator, as well as the concepts behind the implementation.

Equipment

8-1 Multiplexer		4
D Flip-Flop		2
JK Flip-Flop		1
N-Modulo Counter		1
555 Timer		1

Description

The first step of the design process was to design the sequence generator. This required creating a sequence, and then making a next state table based on the sequence. K maps were then created and the necessary connections to each multiplexer were established. The combinational logic was implemented with multiplexers by using the 3 most significant variables as the select lines of the multiplexers, and using 0,1,D and D compliment as the inputs to implement the K-maps. The outputs of the multiplexers were then fed into the flip flops and then back to the input. While the circuit was relatively simple, there was much debugging to be done, such as checking that the combinational logic was correct, that all wires were properly connected, and that the integrated circuits were all functioning properly. The clock was then controlled by a button, and the outputs attached to the bits of a 4 bit LED, so that with each button press, the displayed number changed.

The second aspect of the project was creating a tone generator, and modulating the generated tone with the sequence generator to create a tone sequence. The tone was created with a 555 timer, with resistors and a capacitor attached to tune the frequency to 16 KHz. The next step was using a Modulo N counter, attaching the generated tone to the clock, the sequence generator output to the 4 bit inputs on the counter, and using the Load and ENT pins on the counter to get the modulated frequency. Next, the frequency was divided using a T flip-flop, created by connecting the J and K pins of a JK flip flop both to an input of

1. The modulated frequency was input to the CLK pin on the flip flop, so that the output was a square wave with a frequency of half the input. This output was then attached to a speaker, which included a capacitor to ground. The final result was a repeating sequence of pitches.

Specifications

Combinational logic to be implemented with multiplexers
D flip-flops for sequence generator
555 timer, N-Modulo counter, and JK flip flop to implement frequency generator

Design Synthesis

Truth Table

	A	B	C	D	A^+	B^+	C^+	D^+
S_0	0	0	0	1	0	0	0	0
S_1	0	0	0	0	0	0	1	1
S_2	0	0	1	1	0	0	1	0
S_3	0	0	1	0	0	1	0	1
S_4	0	1	0	1	0	1	0	0
S_5	0	1	0	0	0	1	1	1
S_6	0	1	1	1	0	1	1	0
S_7	0	1	1	0	1	0	0	1
S_8	1	0	0	1	1	0	0	0
S_9	1	0	0	0	0	0	0	1

The truth table gives the output sequence that will be generated based on a given input sequence. It is based on a semi random sequence of notes.

K-Maps

AB/CD	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	0	0	0	0
10	0	1	0	0

$A^+ = A'BCD' + AB'C'D$

AB/CD	00	01	11	10
00	0	1	0	0
01	0	1	0	0
11	0	1	0	0
10	1	0	0	0

$B^+ = A'BC' + A'BD + A'B'CD'$

AB/CD	00	01	11	10
00	1	1	0	0
01	0	0	0	1
11	1	1	0	0
10	0	0	0	0

C^{+} = A'C'D' + AB'C'D +A'CD

AB/CD	00	01	11	10
00	1	1	0	1
01	0	0	0	0
11	0	0	0	0
10	1	1	0	0

D^{+}= BD' + AB'CD'

The K-maps organize the information on the truth table by each output, making it easier to convert the truth table into a diagram for each multiplexer.

0	PA+
0	
0	
D	
D'	
0	
0	
0	

0	PB+
D	
1	
D'	
0	
0	
0	
0	

	PC+
D'	
D'	
D'	
D'	
0	
0	
0	
0	

	PD+
D	
D	
D	
D	
0	
D	
0	
0	

The Multiplexer diagrams lay out the given inputs for each multiplexer based on the truth table and K maps. There is one multiplexer per output.

Answers to the questions in the lab handout

R_A = 2k, R_B = 3.3k, C = 10uF, f_{in} = 16kHz
$t_H = .693(R_A + R_B)C = 36.729$ ns
$t_L = .693(R_B * C) = 22.869$ ns
$T = t_H + T_L = 59.598$ ns
Duty Cycle = $t_H/T * 100 = \%61.62$

With a modulo-4 counter, the output RCO frequency is(1/4+1)*f0 = 16/5kHz

Conclusion

The project in concept was simple but there were a lot of technical difficulties along the way. Errors in calculati wiring, and IC failure all had to be checked for, and the circuit had to be completely redesigned several times. T concepts such as modulo N counters and 555 timers were actually the easiest part of the project to implement. Learning the most efficient methods to debug the project, and to make sure your calculations are perfect before b were the most important lessons of this project.

Works Cited

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