Digital Design Lab
EEN 315 Section 47

Lab 2: Three-bit Loadable Up-Down Synchronous Counter Attached to a 7 – Segment display and a Sequence Detector

DigiD's 2012
Connor Akio McCullough III
(Partners: Anthony Taboada
Joe Barra
Davis Sprague)

May Lin, TA

University of Miami
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Abstract

The purpose of this lab was to design and implement an incrementor and decrementor which will increment in steps of one. The load line control switches to a seven segment display. The incrementation process is implemented only using 8:1 multiplexers. The direction of counting is done with an additional input switch. The 3 bits display the digits 1 through 7 and the switch allows the user to decide whether to count up or down. The load line is used to override the counter and allow the user to input numbers zero through seven using binary switches.

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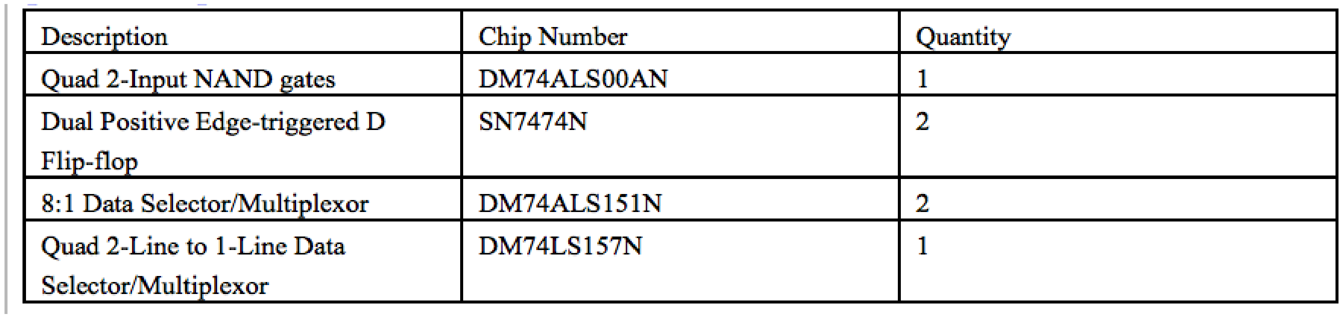
Overview

This lab tested understanding of multiplexors especially for implentation of basic counting. Also, ability to implement multiple state machines at once and functioning as a cohesive circuit is neccesary. Knowledge of basic Boolean algebra, flip flops, and NAND gates was neccesary as well.

Objectives

The objective of this lab was to implement multiplexers in a digital circuit, and to use the multiplexer to switch between two different digital circuits.

Equipment



Description	Chip Number	Quantity
Quad 2-Input NAND gates	DM74ALS00AN	1
Dual Positive Edge-triggered D Flip-flop	SN7474N	2
8:1 Data Selector/Multiplexor	DM74ALS151N	2
Quad 2-Line to 1-Line Data Selector/Multiplexor	DM74LS157N	1

Description

The first step of the project was to create truth tables for the multiplexers for use in the up and down counters. Use of K-Maps allowed the project to be simplified from three multiplexors to two. The final implementation called for a three bit input at the select line and up down switch as the input. The U/D input of '1' would increment the counter and '0' would decrement it.

For counting and displaying the seven segments, an 8:1 multiplexer was needed to display 0-7, which is seven different states. The outputs of these would go into the 2:1 multiplexer which was used to switch between counter and manual input.

The output of these 2:1 multiplexers leads into the D-flip flops, which goes to the seven segment display and back to the select lines of the multiplexer.

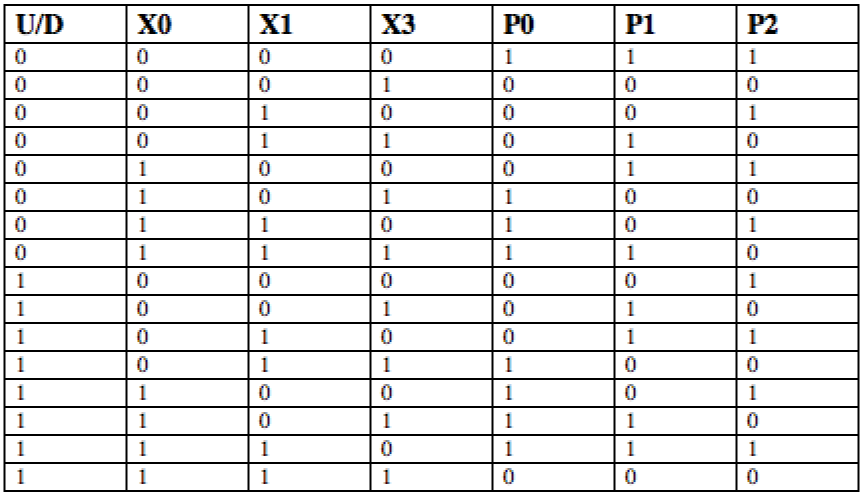
For a correct output to be returned with only 3 bits used, the fourth had to be grounded, which is the most significant bit since the numbers used do not go above 7. The G pin on the multiplexers also always has to be grounded, and the CLR and PRE on the flip flops must be set to high.

Specifications

Only NAND gates could be used for the seven segment display. There could only be one Quad 2:1 Multiplexer for the up/down and loadable counter, and two 8:1 multiplexers with 2 D flip flops.

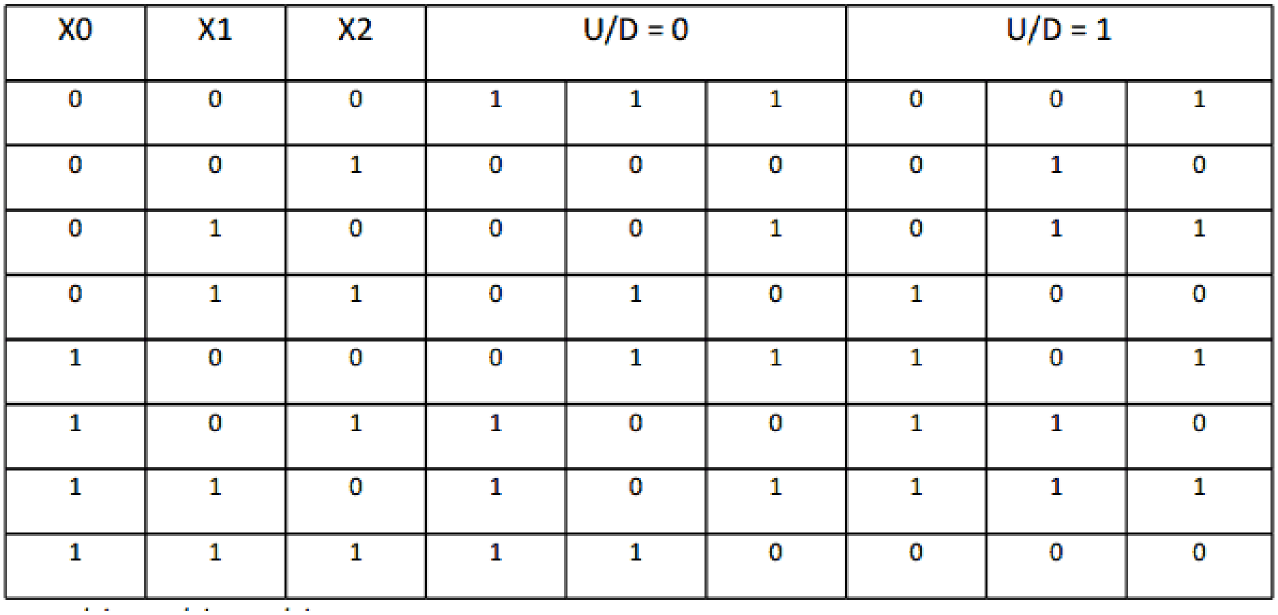
Design Synthesis

Truth Table:



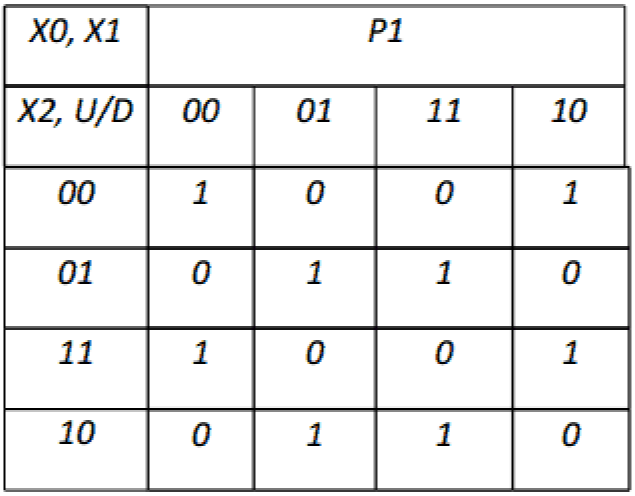
U/D	X0	X1	X3	P0	P1	P2
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	1
0	1	0	1	1	0	0
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	1
1	0	1	1	1	0	0
1	1	0	0	1	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1
1	1	1	1	0	0	0

Next State Table:

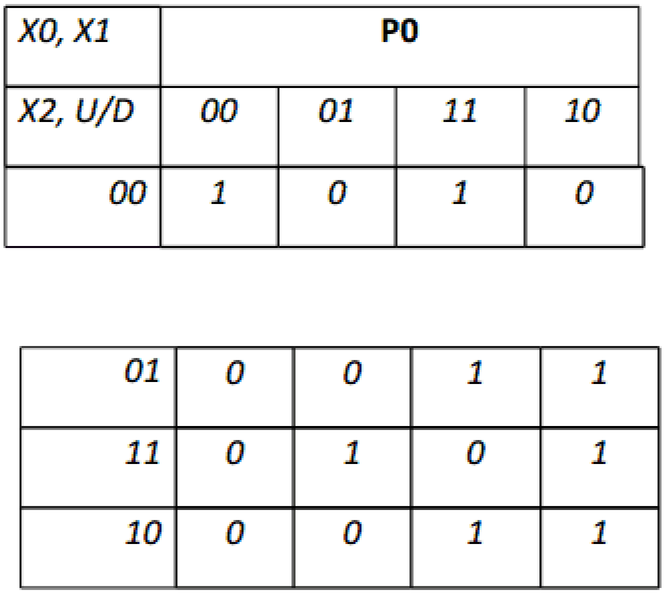


X0	X1	X2	U/D = 0			U/D = 1		
0	0	0	1	1	1	0	0	1
0	0	1	0	0	0	0	1	0
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	1	0	0
1	0	0	0	1	1	1	0	1
1	0	1	1	0	0	1	1	0
1	1	0	1	0	1	1	1	1
1	1	1	1	1	0	0	0	0

K-Map (Part A):



X0, X1	P1			
X2, U/D	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	1	0	0	1
10	0	1	1	0



X0, X1	**P0**			
X2, U/D	00	01	11	10
00	1	0	1	0
01	0	0	1	1
11	0	1	0	1
10	0	0	1	1

X0, X1	P2			
X2, U/D	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	0	0	0	0
10	0	0	0	0

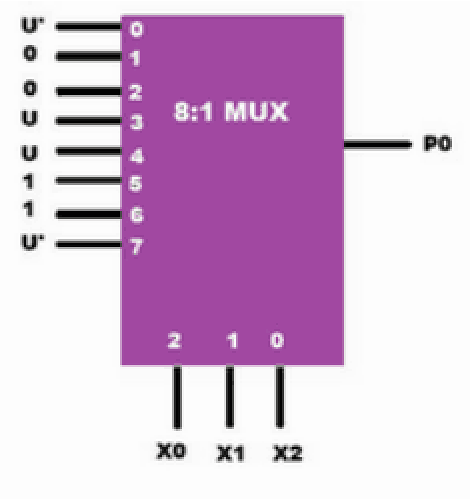
Equations:

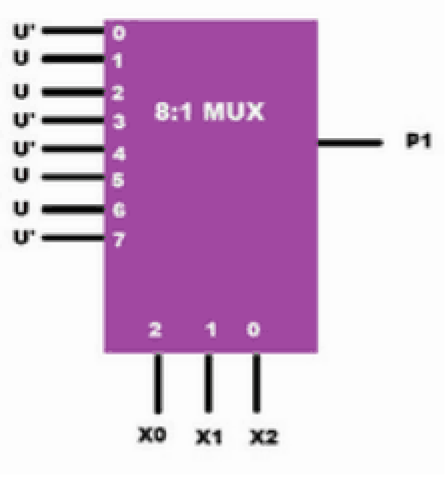
$P_0 = X'_0X'_1X'_2U' + X_0X_1U' + X_0X'_2U + X_0X'_1X_2$

$P_1 = X'_1X'_2U' + X_1X'_2U + X'_1X_2U + X1X_2U'$

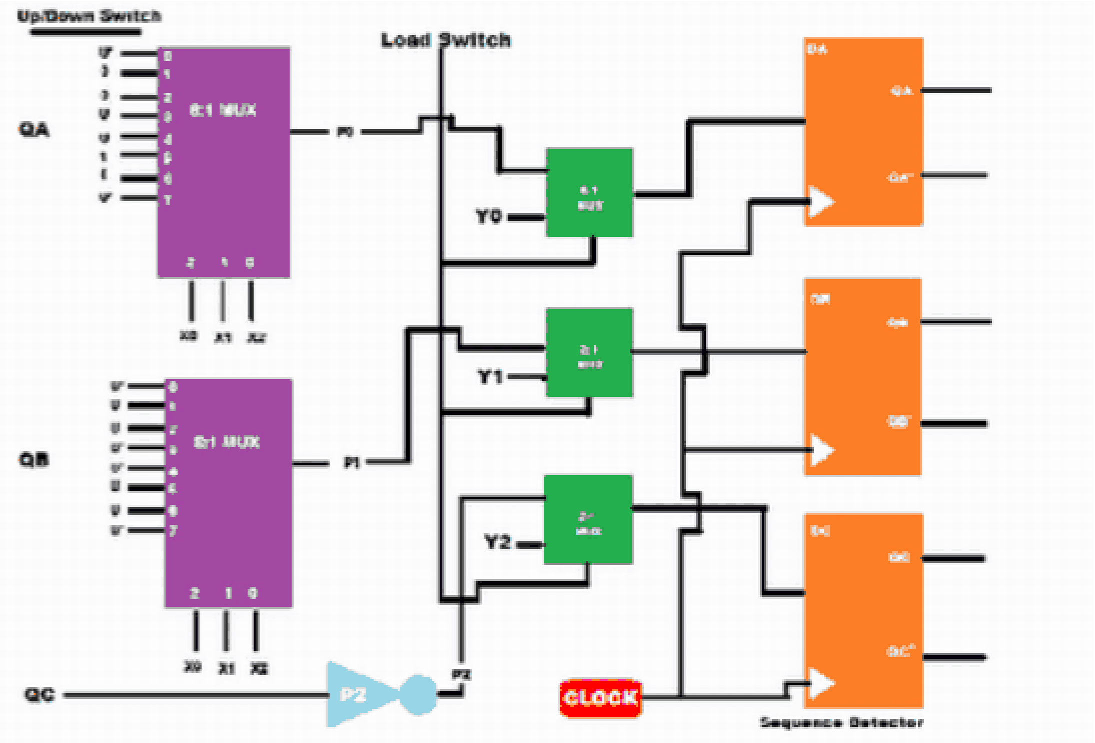
$P_2 = X'_2$

Multiplexer Design:

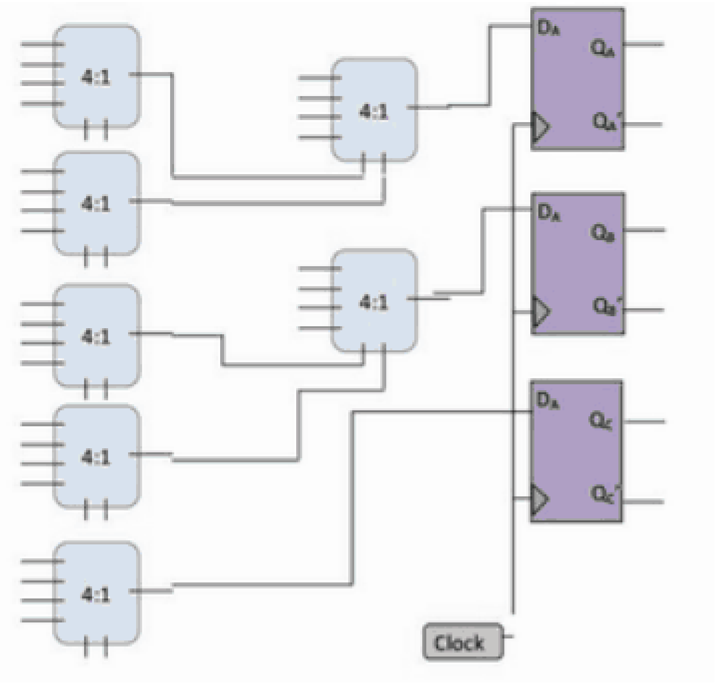


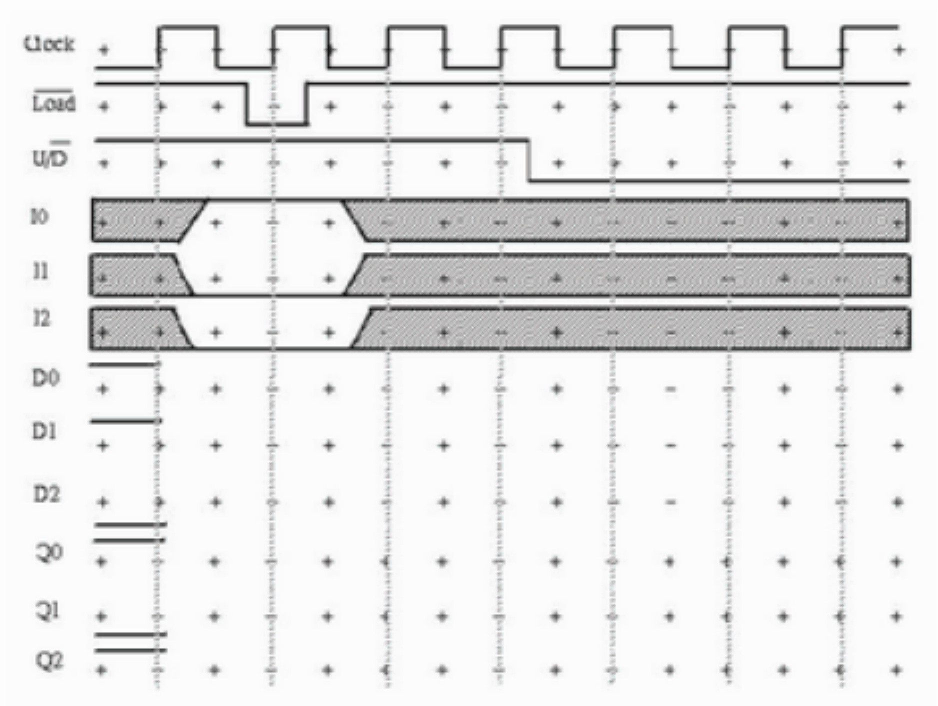


Complete Logic Diagram



Answers to the questions in the lab handout


4:1
4:1
4:1
4:1
4:1
4:1
4:1
D_A
Q_A
Q_A'
D_A
Q_B
Q_B'
D_A
Q_C
Q_C'
Clock


Clock
Load
U/D
I0
I1
I2
D0
D1
D2
Q0
Q1
Q2